NOPE: Normally-Off Platforms for Embedded systems

IETR/SysCom
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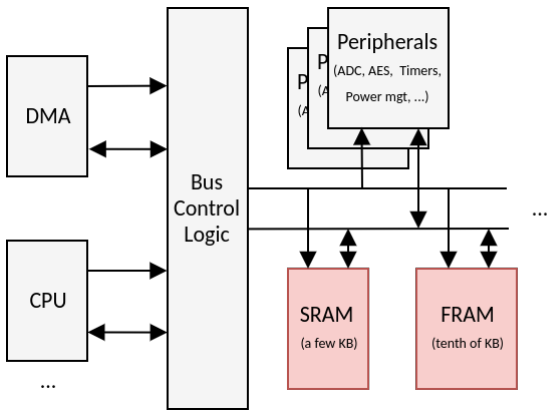
From normally-off computing to transient computing

Normally-off computing is a design paradigm targeted towards decreasing as much as possible the energy consumption of a system while maintaining a minimum quality of service, especially through power gating. This approach has importantly benefited from the emergence of **new non volatile memory technologies** based on spintronic.

In the context of embedded systems/IoT, normally-off computing has been used to build **battery-less sensor nodes** powered by supercapacitors connected to one or more ambient **energy harvesting** devices.

Based on the same set of technologies, **transient computing** aims at reconciling normally-off computing with edge/near-sensor computing. Therefore, it raises the problem of **running computation on a device that is connected to an intermittent power source**.

Architecture of current micontroller integrating emerging NVM technologies



For a few years, small MCUs have been shipping with FRAM modules instead of Flash.
In these systems, SRAM is still used as the main working memory because it is faster and has lower dynamic energy consumption.
FRAM can be used as a drop-in replacement for Flash, but its **performance also offers new opportunities that are game changing for transient computing.**

Impact of emerging Non Volatile Memory technologies

	SRAM	Flash	STT-MRAM	FRAM
Cell Size (F^2)	120-200	4-6	6-50	6-40
Write cycles	10^{16}	10^4-10^5	10^{12}-10^{15}	10^{14}-10^{15}
Read latency	0.2–2 ns	15 – 35 µs	2 – 35 ns	20 – 80 ns
Write latency	0.2–2 ns	200 – 500 µs	3 – 50 ns	50 – 75 ns
Leakage power	High	Low	Low	Low
Dyn. energy (R/W)	Low	Low	Low / High	Low / High

Main performance figures of emerging NVM[1].

[1] J. Boukhobza *et al*. Emerging NVM: A Survey on Architectural Integration and Research Challenge. ACM Trans. Design. Autom. Electr. Syst., 23(2), 2017

Performance of emerging non volatile memory technologies like STT-MRAM of FRAM brings **fast and energy efficient checkpointing of the volatile state of the system accross power losses** to small embedded systems.
In a transient system, this property opens the door to **the capacity to run long computations that spread accross several power cycles.**

Computing on a transient platform

Programmers are not used to deal with power losses, so do their programs. Ideally, the **execution model should thus provide abstractions to handle power losses as a normal event**, not as a system failure.

For **computation intensive tasks** whose execution spreads accross power cycles, an **automated checkpointing and rollback** mechanism must be used. Then:

- How to ensure progress accross power cycles?
- How to enforce correctness (idempotent execution)?

For **I/O intensive / reactive tasks** or for small tasks that fit in a power cycle, **atomicity wrt. power failures** must be enforced. Then:

- How to evaluate the energy consumption of a task?
- How to minimize the amount of lost cycles?

Scientific program and main achievements

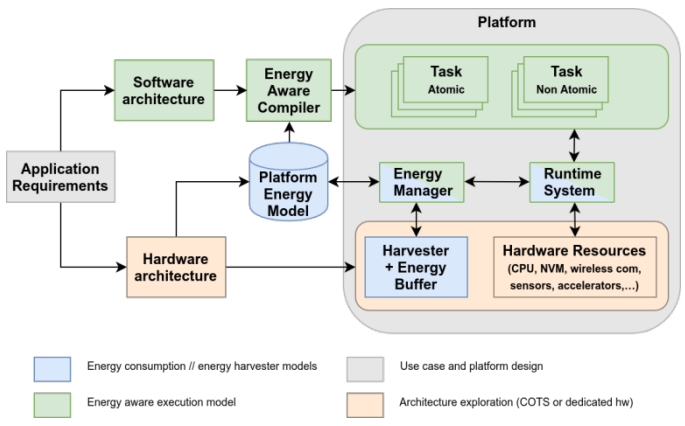
Exploratory action NOPE did gather skills in compilation, architecture, runtime systems and embedded systems, with the following goals:

- Building and sharing a strong expertise in transient computing and **identifying challenges**.
- Initiating collaborations between the members of the consortium.
- Building the foundations of a **shared experimental platform** for transient computing.

The following goals have been achieved:

- Start the development of a shared experimental platform based on TI MSP430FR5969 FRAM MCU.
- Port of Trampoline RTOS to the platform.
- Port of Heptane static WCET/WCEC analyzer for the platform.
- Evaluation of S-o-t-A solar harvesting prediction algorithms

Our vision: towards a safe and efficient transient computing platform



Summary

Transient computing wants to reconcile normally-off and near-sensor computing.
Thus, execution platform shall seamlessly handle power losses.
We aim at building such platforms by leveraging advanced software (compilation, runtime) and hardware (architecture, energy management) technologies.