Scratchy – A lightweight Scratchpad-Based Multi-RISC-V

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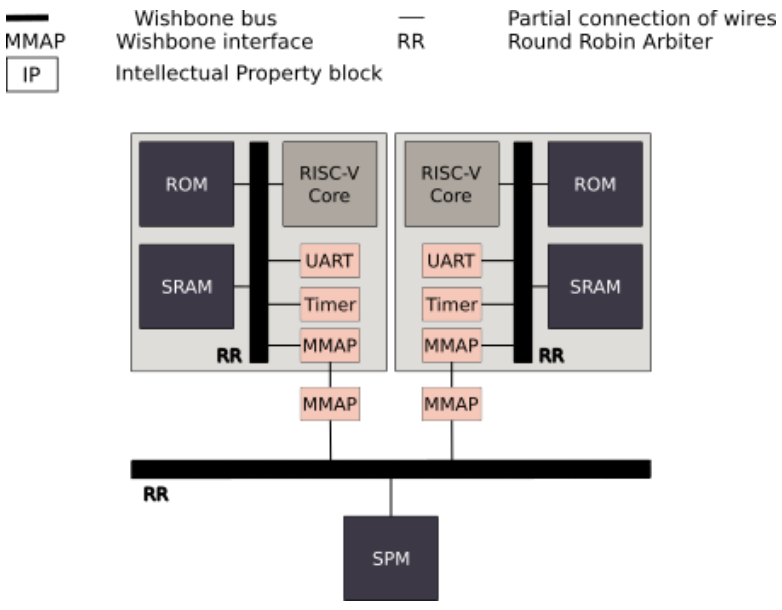
Adapting the architecture to the needs of a streaming application

- Caches are inefficient for streaming applications with process-and-forget data nature [G22].
- Scratchpad memories (SPM) i.e. small and fast shared memories, can be employed to hold computing results and distribute data in a multiprocessor [R19]
- Scratchy aims at **tailoring computing resources** of a multiprocessor to the **needs of a Synchronous Dataflow (SDF)** modeled application.

Scratchy structure and its lightweight nature

- Scratchy is **lightweight**, with little overhead for inter-processors communication.
- A 2-core Scratchy fits a DE10-lite MAX10 Intel FPGA,consuming less than 30% of logical elements.



	Comb. Func. (CFs)	Registers (REGs)	CFs overhead	REGs overhead
FireV SoC	2308	1047	-	-
FemtoRV SoC	1700 (3%)	759	-	-
2coreScratchy (Firev)	5029 (10%)	2146 (4%)	+413(+8.9%)	+52(+2.5%)
2coreScratchy (FemtoRV)	3837 (8%)	1570 (3%)	+437(+12.8%)	+52(+3.4%)

Scratchy Characteristics

- Scratchy is **Migen** HDL and **Litex** [K19] based.
- Core types, memory sizes and distributivity, bus connectivity is **customizable**. Current implementation supports FireV and FemtoRV RISC-V cores.
- A 4-Core Scratchy is synthetised in **less than 3 minutes**.

References

[G22] Ghasemi et al.(2022). The Impact of Cache and Dynamic Memory Management in Static Dataflow Applications. Journal of Signal Processing Systems, 94(7), 721-738.
[K19] Kermarrec, et al. DATE'19. LiteX: an open-source SoC builder and library based on Migen Python DSL. Workshop on Open Source Design Automation (OSDA),
[R19] Rouxel, et al. (2019). Hiding communication delays in contention-free execution for spm-based multi-core architectures. In 31st Euromicro Conference on Real-Time Systems (ECRTS 2019).
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