EPFL-Inria
INTERNATIONAL LAB

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Inria
INVENTEURS DU MONDE NUMÉRIQUE

Workshop EPFL-Inria
January 9 and 10, 2020, Montbonnot

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Title: « On compilers for FPGA accelerators »

Abstract:

Since the end of Dennard scaling, power efficiency is the limiting factor for large-scale computing. Hardware accelerators such as reconfigurable circuits (Field-Programmable Gate Array, FPGA) or Graphics Processing Units (GPUs) were introduced to improve the performance under a limited energy budget, resulting into complex heterogeneous platforms. FPGAs are a credible solution to reach the energy efficiency levels required by big data and deep learning applications...at the price of designing a circuit configuration. Hence the need for high-level programming tools (High-Level Synthesis, HLS).
In this talk, we will discuss some of our contributions for compiling high-level programs to FPGA accelerators. In particular, we will present a compilation scheme for parallelizing C programs and synthesizing the control and the data transfers to an FPGA circuit configuration.