Maximize energy efficiency in a normally-off system using NVRAM

- *Stéphane Gros*
- *Yeter Akgul*

Summary

THE COMPANY

THE CONTEXT

THE TECHNOLOGY

THE SYSTEM

THE CO-DEVELOPMENT

CONCLUSION

Summary

THE COMPANY

THE CONTEXT

THE TECHNOLOGY

THE SYSTEM

THE CO-DEVELOPMENT

CONCLUSION

spintec
SPIN IN ELECTRONICS

Lab spin-off

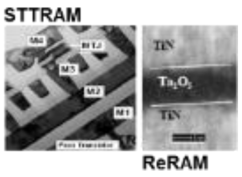
September
Labor Day
5

Incorporated 2014

17 people (14 technical)

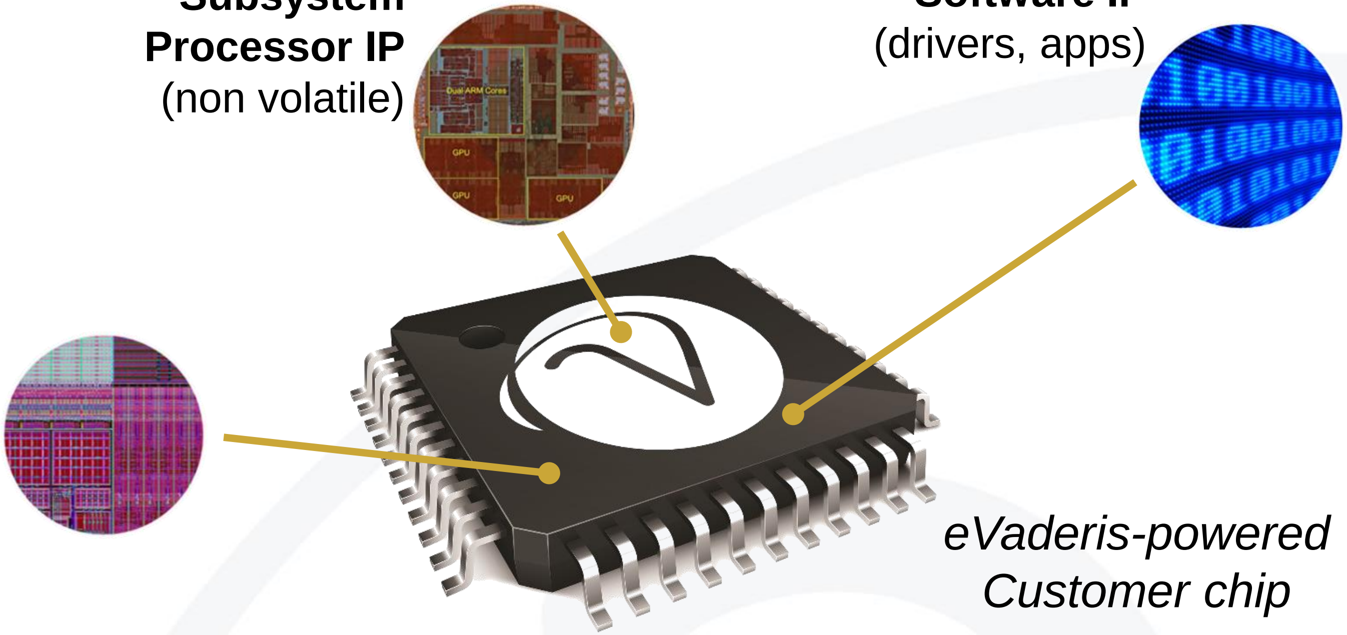
IP Fabless

Non volatile Semiconductor IP



eSTTRAM
(eMRAM)
eReRAM
(eRRAM)

Value proposition



Subsystem Processor IP
(non volatile)

Software IP
(drivers, apps)

Memory IP
(non volatile compilers)

eVaderis-powered Customer chip

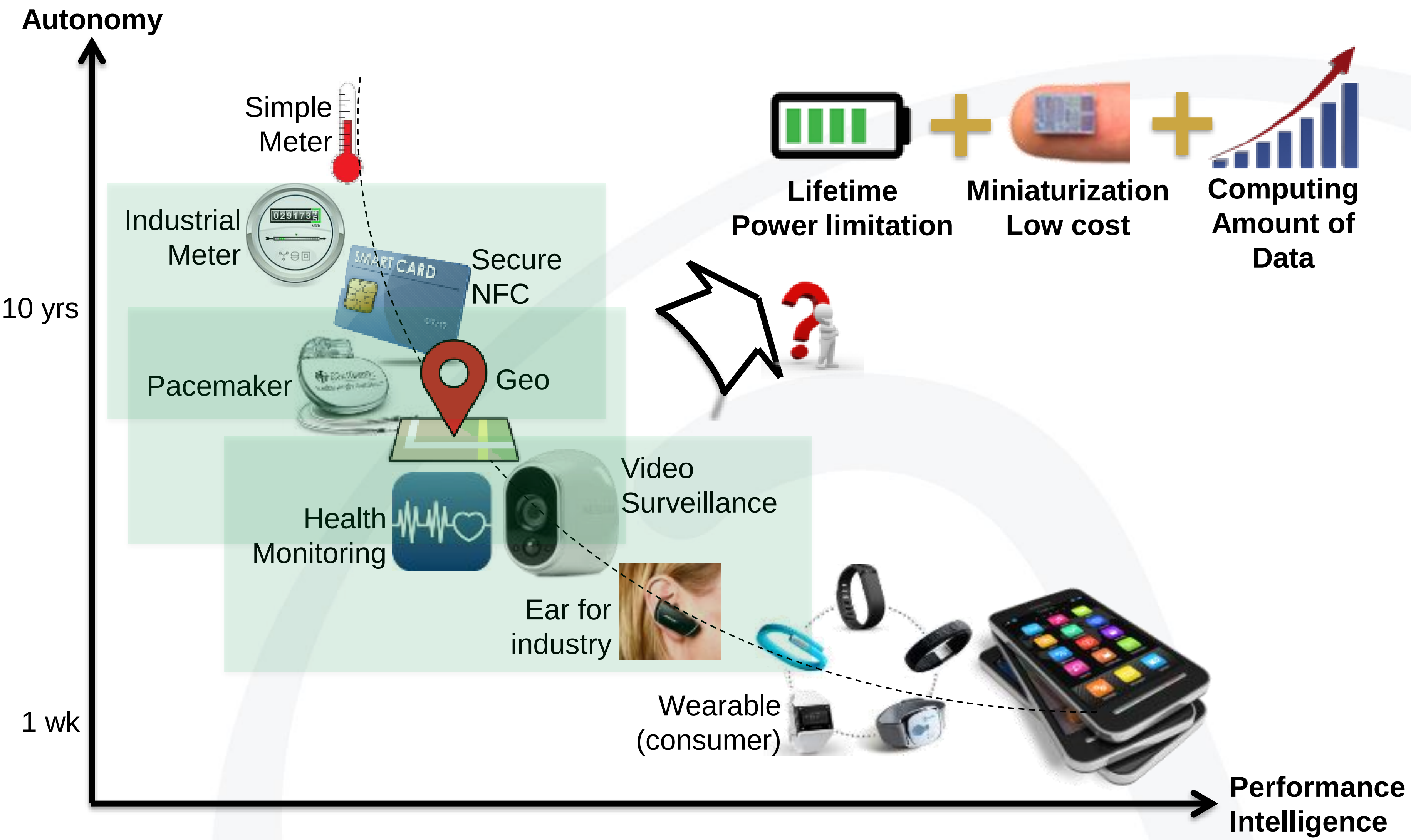
INTELLECTUAL PROPERTY ★ PATENTED ★ INTELLECTUAL PROPERTY

↓**Power**
(active & standby)

↑**Flexibility**
(hardware & software)

↓**Costs**
(density & process)

Positioning



Autonomy

10 yrs

1 wk

Performance Intelligence

Simple Meter

Industrial Meter

Secure NFC

Pacemaker

Geo

Health Monitoring

Video Surveillance

Ear for industry

Wearable (consumer)

Lifetime
Power limitation

Miniaturization
Low cost

Computing
Amount of
Data

Summary

THE COMPANY

THE CONTEXT

THE TECHNOLOGY

THE SYSTEM

THE CO-DEVELOPMENT

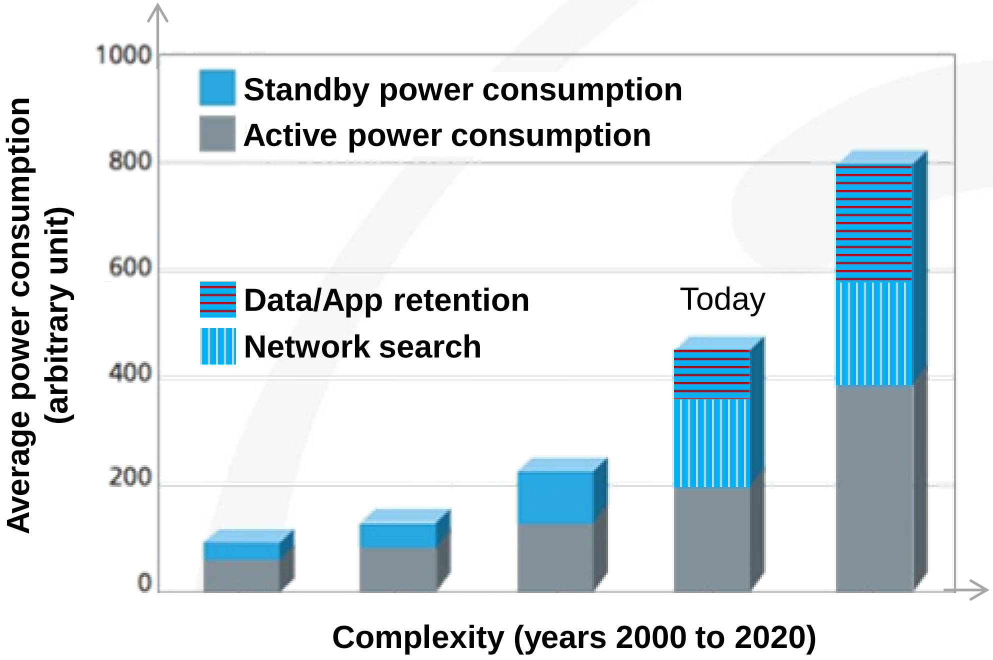
CONCLUSION

The issue

10% active
90% standby

Performances
(computing, amount of data)

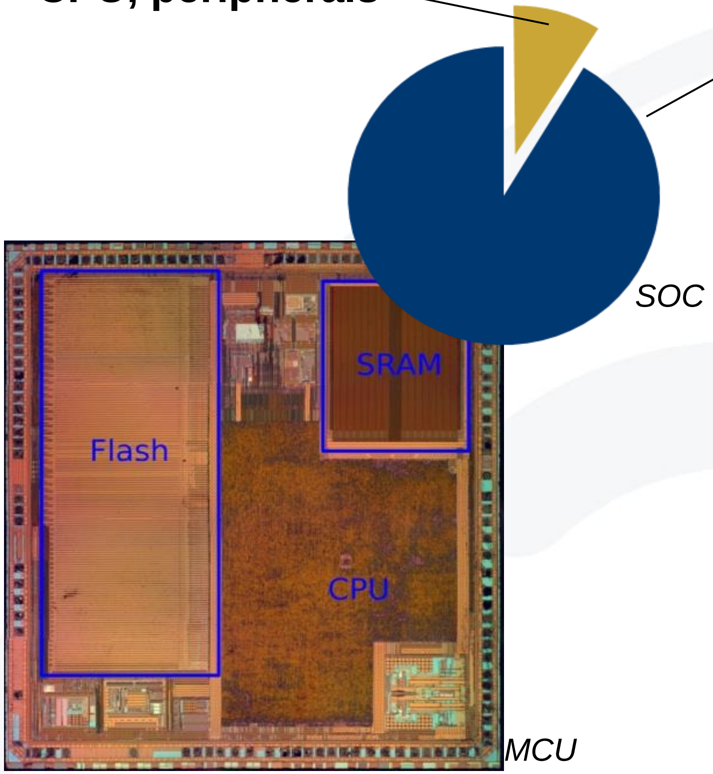
Autonomy
(battery life)



Cell phone dilemma

Increasingly powerful but …
… less and less portable !

MCU level



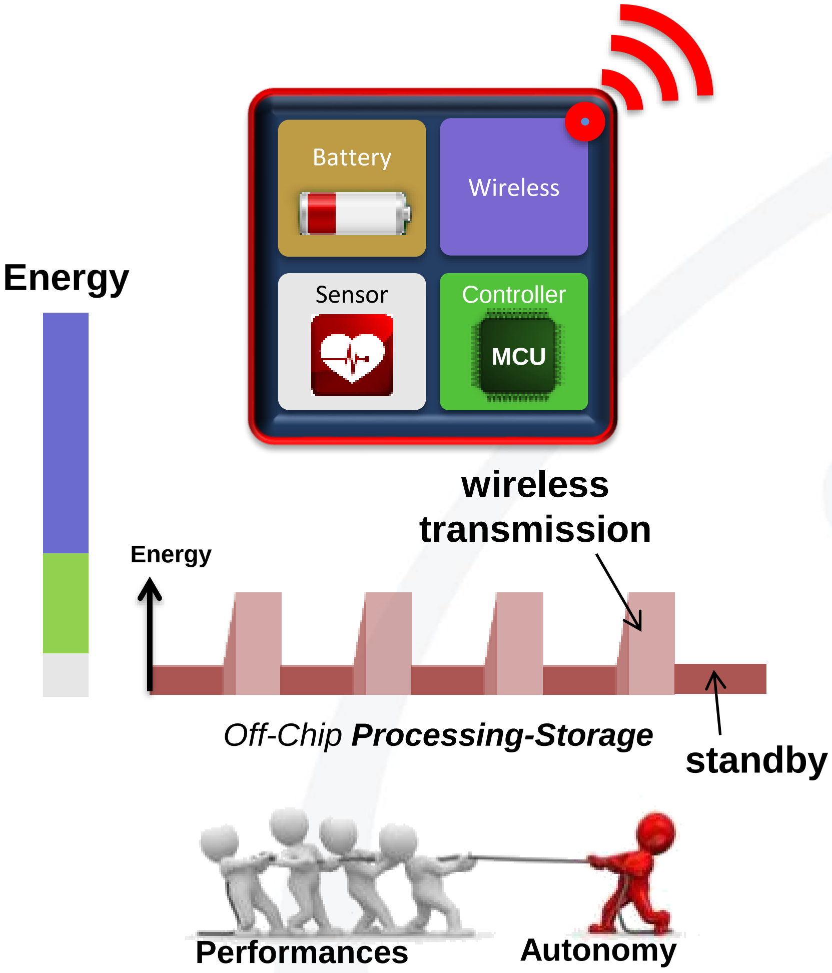
CPU, peripherals

Memories, up to 96% of area, 50% of power consumption for advanced designs

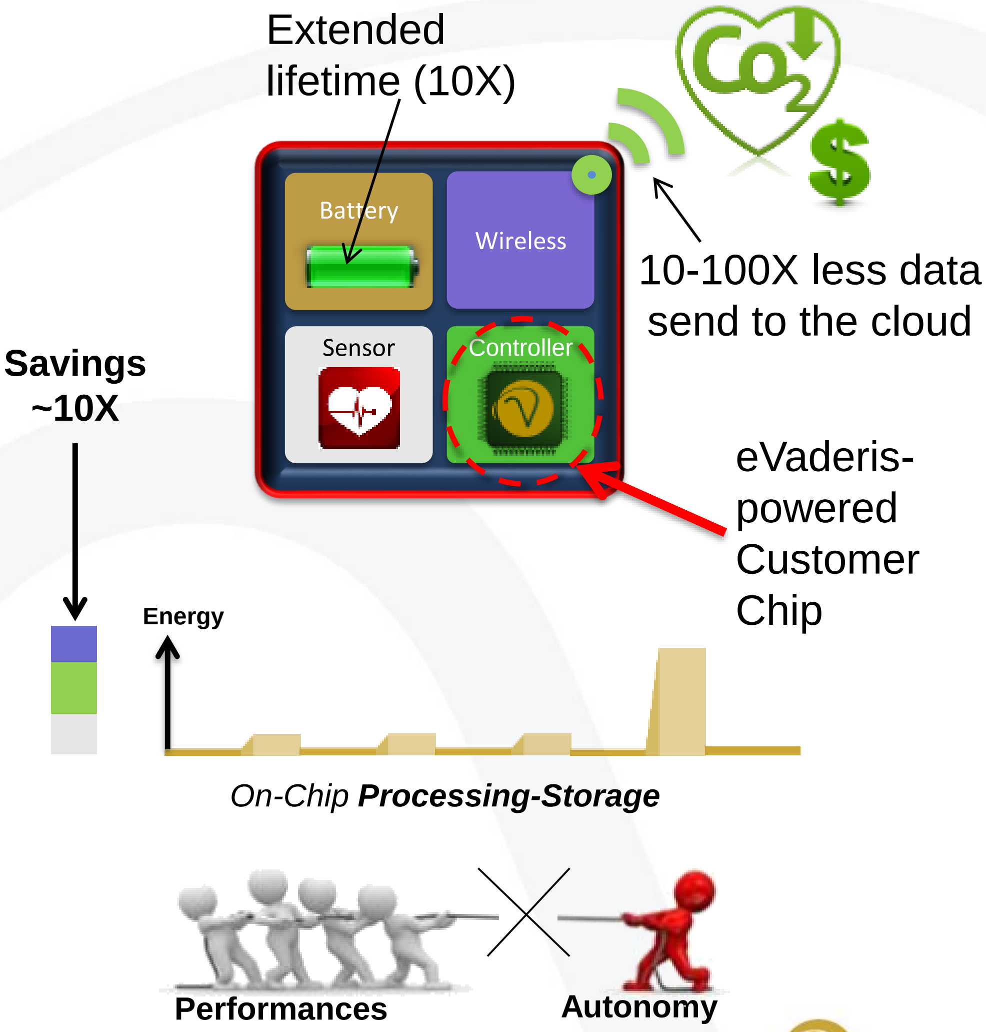
Costly And Complex

Board level

Connected Object
State of the art



Connected Object
Powered by eVaderis


Extended lifetime (10X)

10-100X less data send to the cloud

Savings ~10X

eVaderis-powered Customer Chip

Summary

THE COMPANY

THE CONTEXT

THE TECHNOLOGY

THE SYSTEM

THE CO-DEVELOPMENT

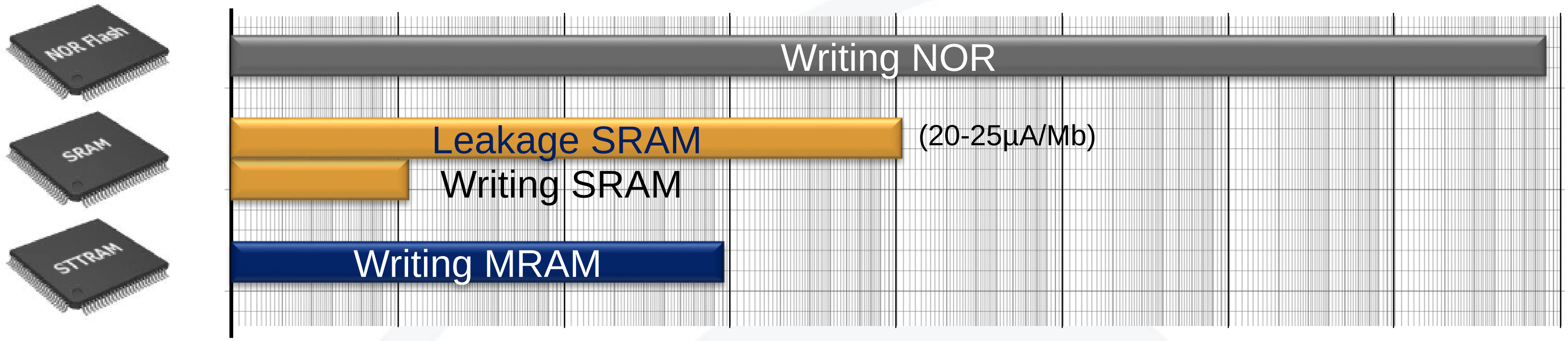
CONCLUSION

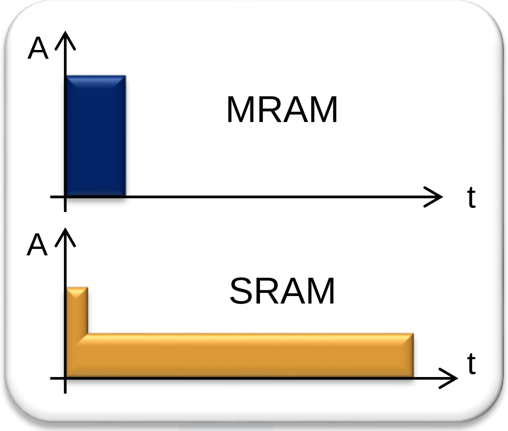
Memory comparison 1/3

	eFlash/eEE	eSRAM	eSTTRAM	eRRAM (Ox)
Non-volatile	Yes	No	Yes	Yes
Compatible with front end logic	☹ No FinFET, FDSOI	Yes	Yes	Yes
Scalable	Sub-28nm ?	Yes (size?)	Yes	Yes
Cell size (density F2)	10-30 (>30 for eEE)	60-80 (HD/LP)	10-30	10-20
Access time	10-100ns (not destructive)	<1ns (not destructive)	2-10ns (not destructive)	10ns (not destructive)
Write/erase process	byte/block/page level	bit level	bit level	bit level
Write/erase time	1us/10ms (erase) (page, byte level)	<1ns	2-10ns (bit level)	10-50ns (bit level)
Endurance	10^5-10^6	>10^{16}	10^{10}-10^{15}	10^7-10^9
Array standby current	0	1-10µA/Mb(25C)	0	0

Memory comparison 2/3

- Storage energy @ constant data (1Mb/1s)



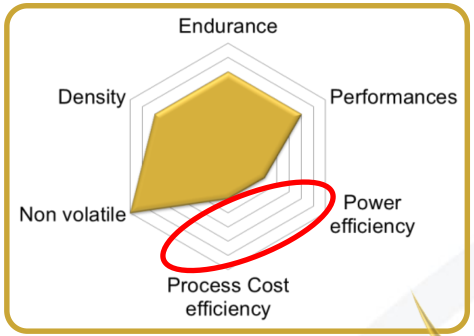


- MRAM vs. SRAM:
  - 100x more energy for writing in MRAM
  - 0 leakage at standby mode (MRAM off)
  - ~4x less area MRAM

Memory comparison 3/3

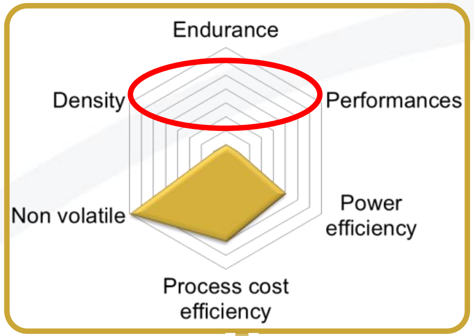
eNOR FLASH/EE

SST CYPRESS PERFORM SPANSION™



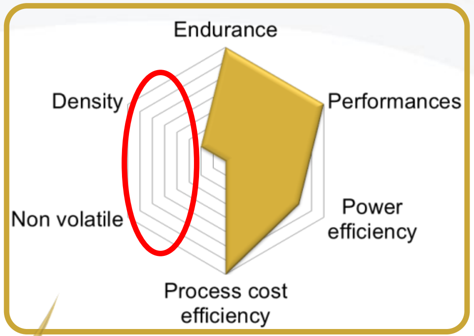
OTP/MTP

SYNOPSYS® Kilopass Sidense

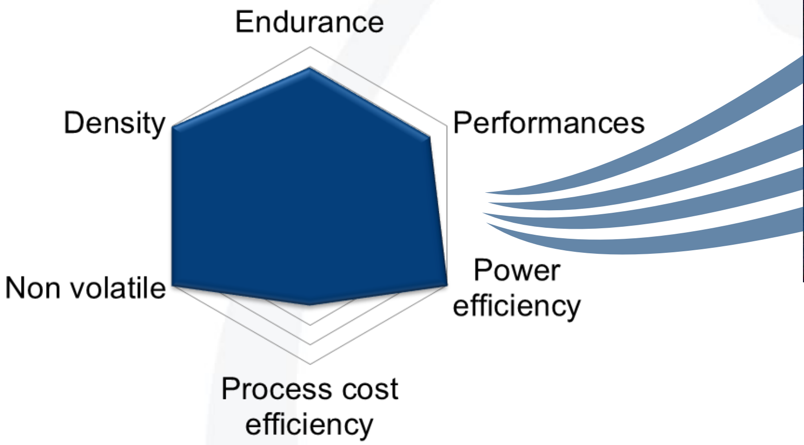


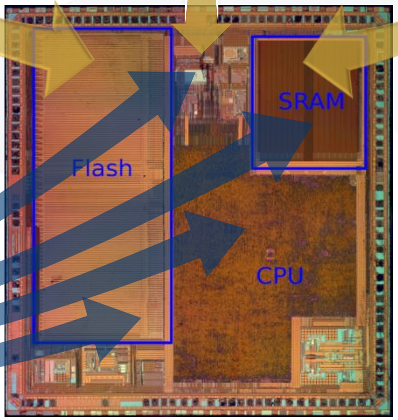
eSRAM/CMOS

SYNOPSYS® ARM eSilicon®

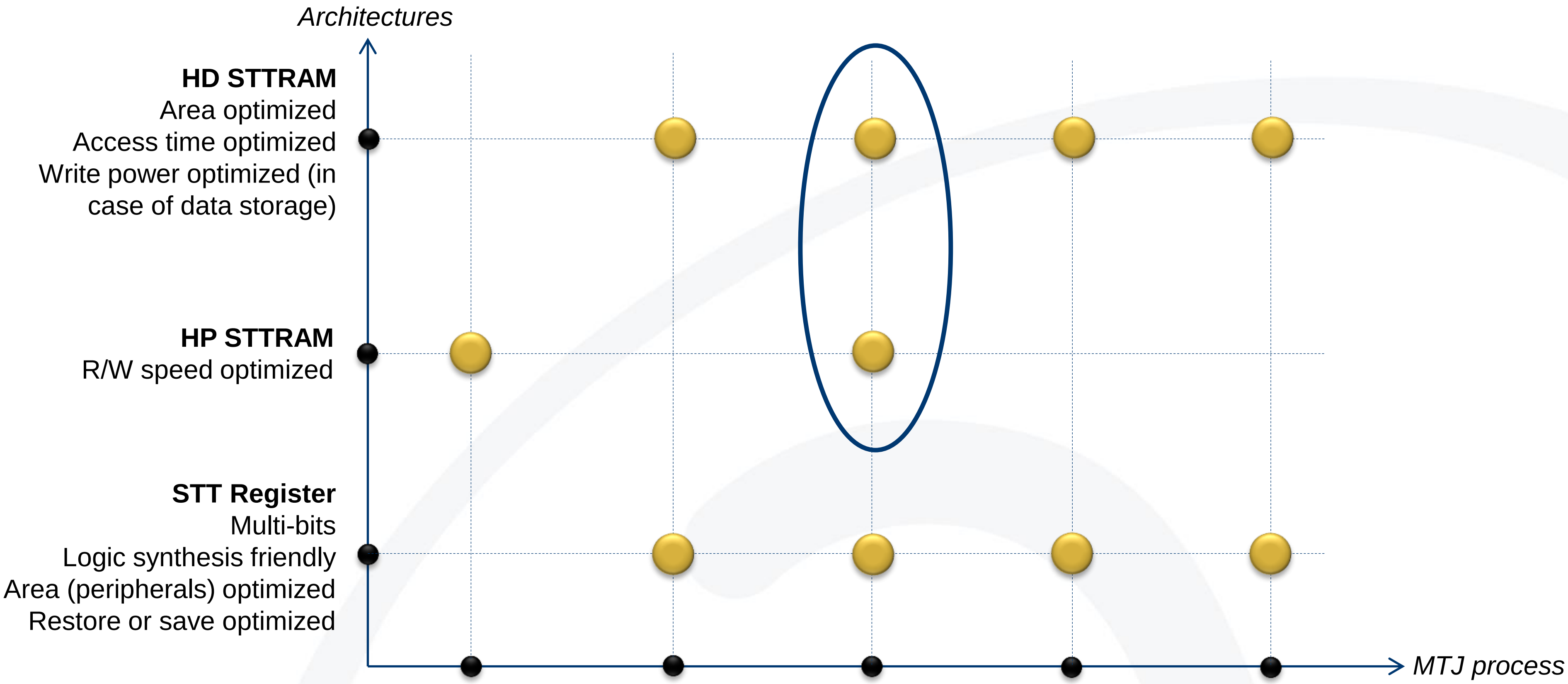


Versatile eSTTRAM





STT-RAM Design Space



HD STTRAM
Area optimized
Access time optimized
Write power optimized (in case of data storage)

HP STTRAM
R/W speed optimized

STT Register
Multi-bits
Logic synthesis friendly
Area (peripherals) optimized
Restore or save optimized

MTJ process	Fast/LP Write	Fast/LP Read	Nominal	Med Ret/T°	High Ret/T°	
Diameter (sizing)	LOW	LOW	LOW	LOW	HIGH	*(design param.)*
Retention (Ic)	LOW	MED	MED	HIGH	HIGH	
Planar polarizer	YES	MED	MED	NO	NO	
Damping	LOW	MED	MED	HIGH	HIGH	
RA/TMR	LOW	HIGH	MED	HIGH	MED	

Many process and architectures tradeoff are possible

Summary

THE COMPANY

THE CONTEXT

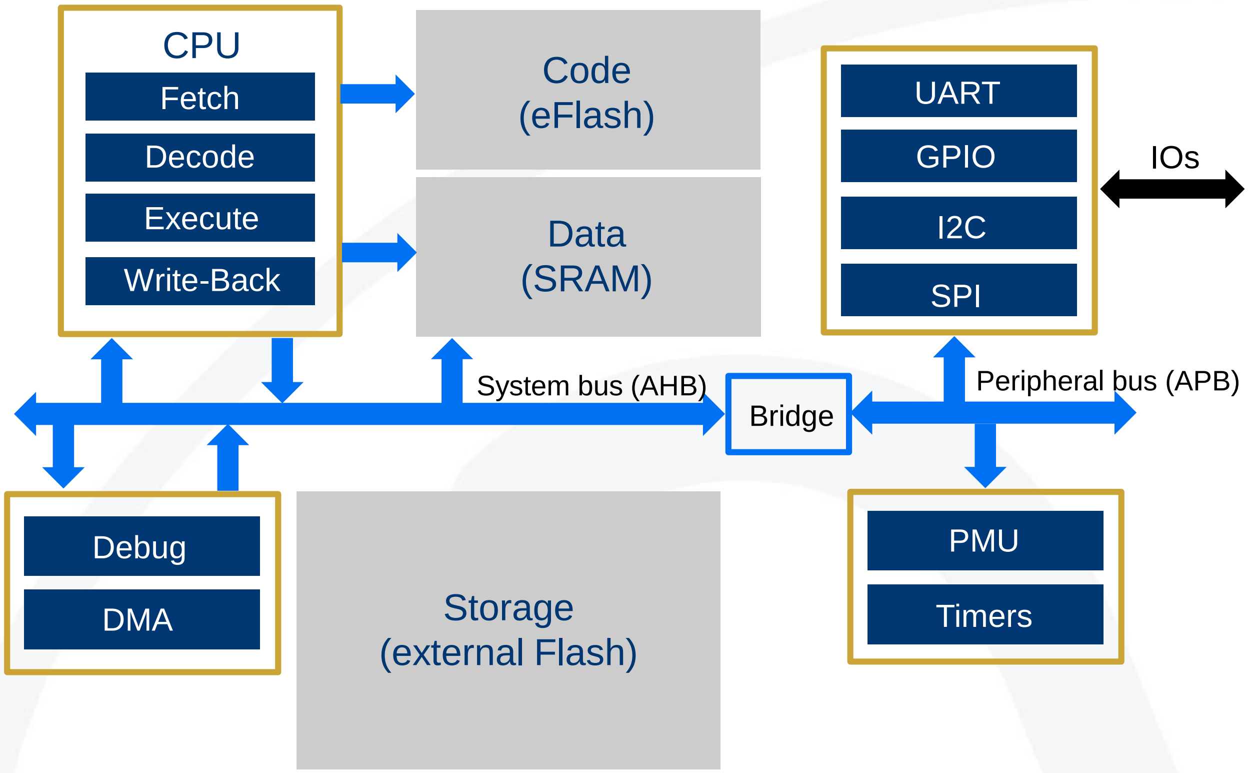
THE TECHNOLOGY

THE SYSTEM

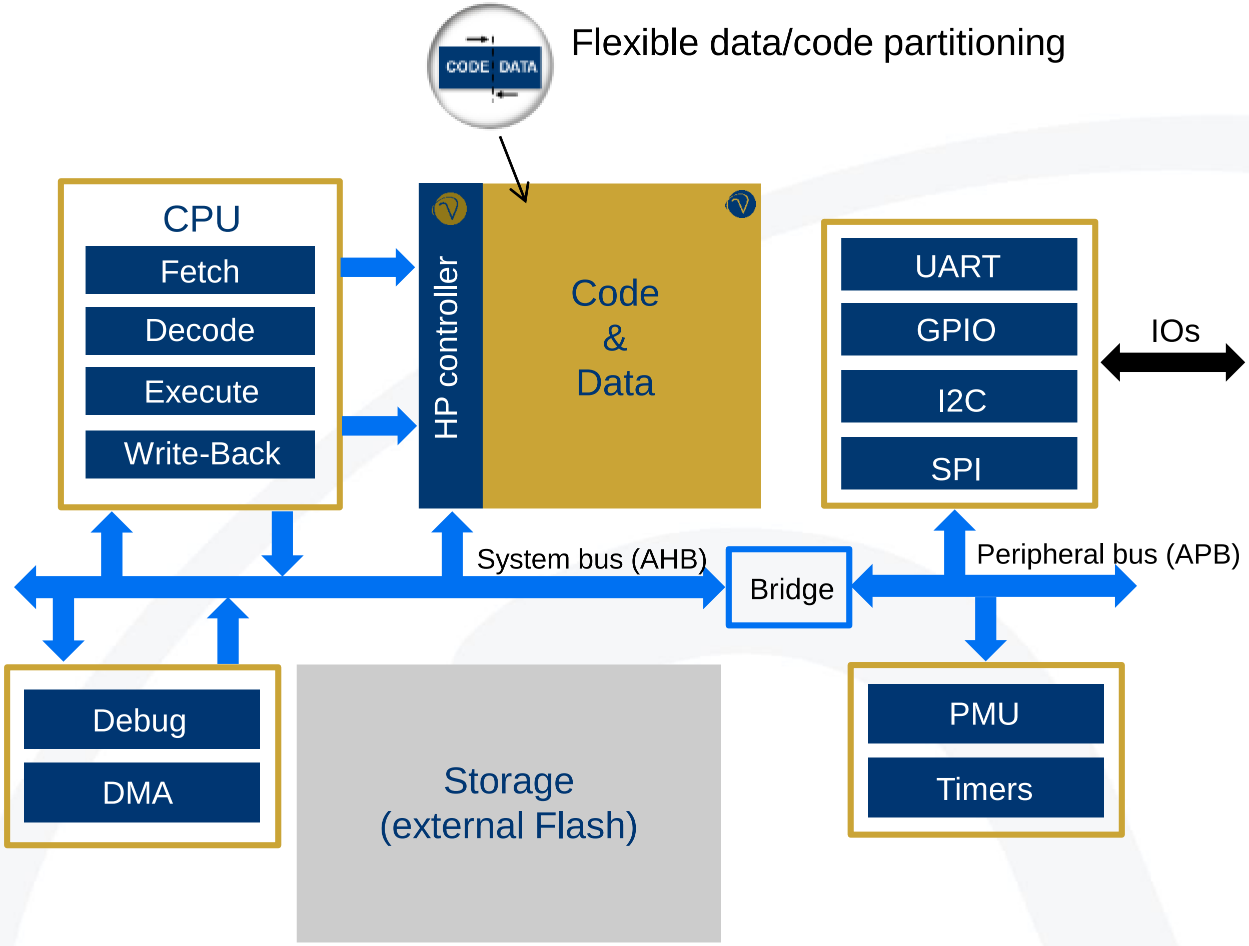
THE CO-DEVELOPMENT

CONCLUSION

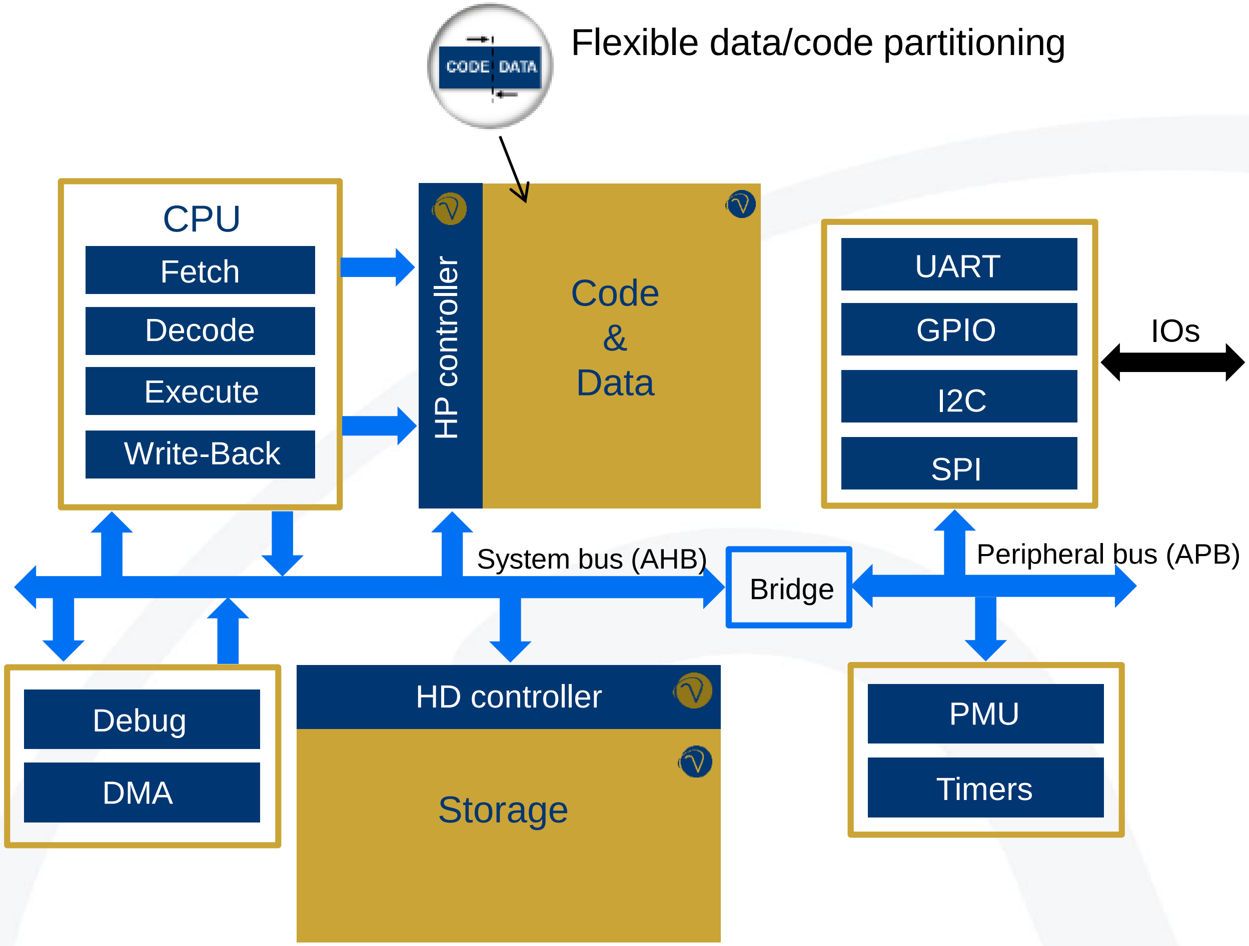
Non-Volatile System



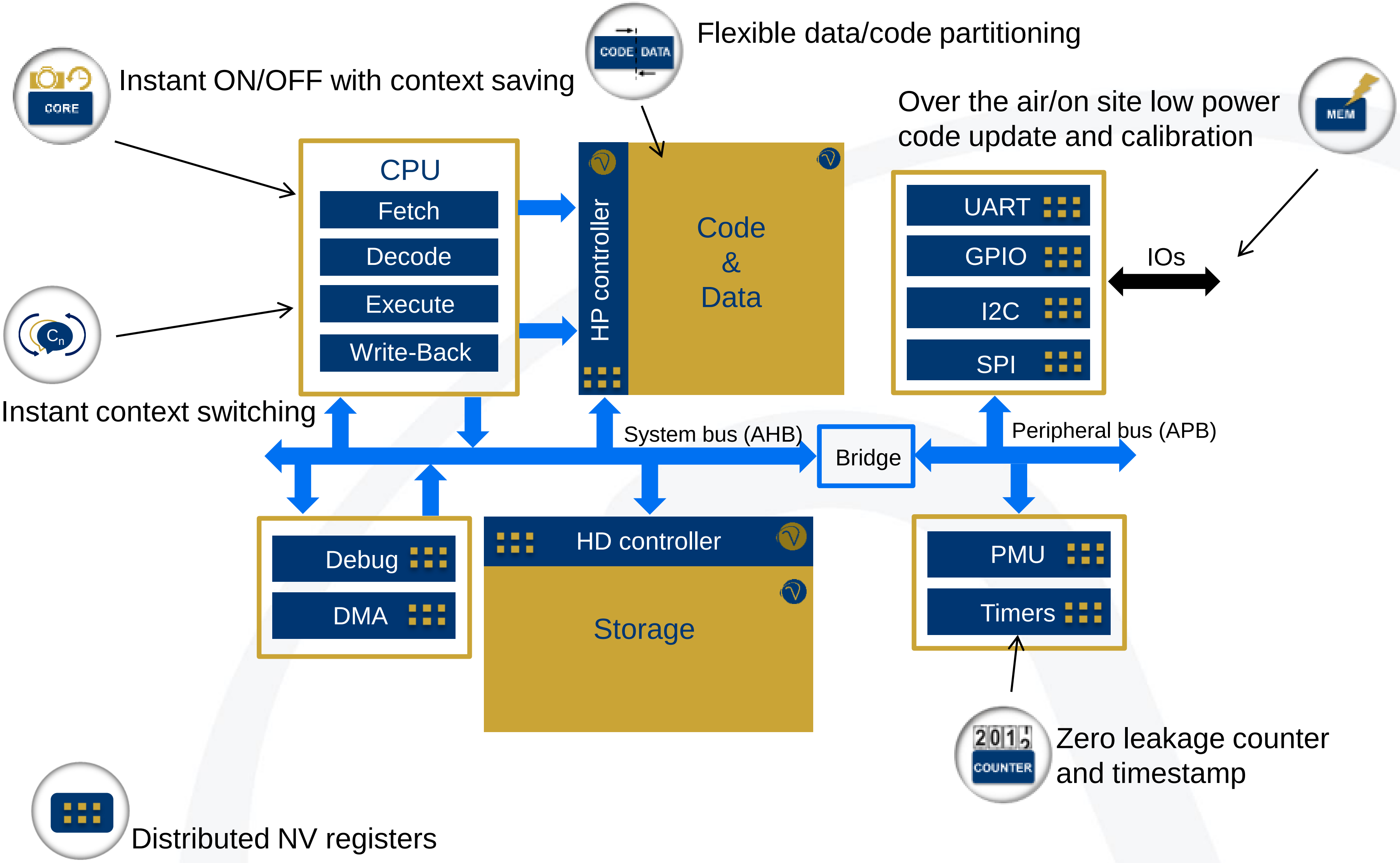
Non-Volatile System



Non-Volatile System



Non-Volatile System



Instant ON/OFF with context saving

Flexible data/code partitioning

Over the air/on site low power code update and calibration

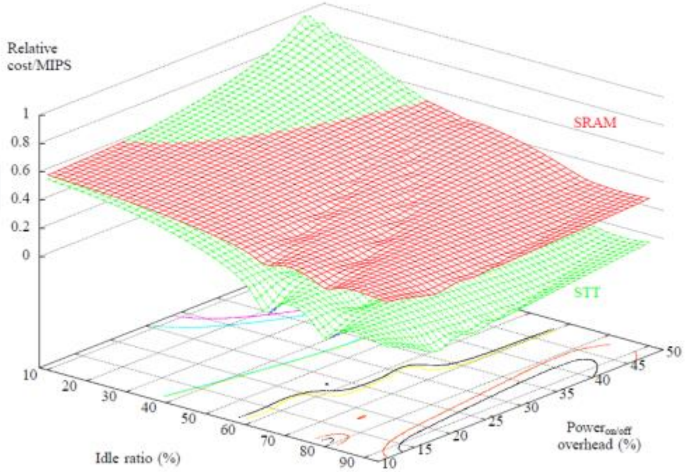
Instant context switching

Zero leakage counter and timestamp

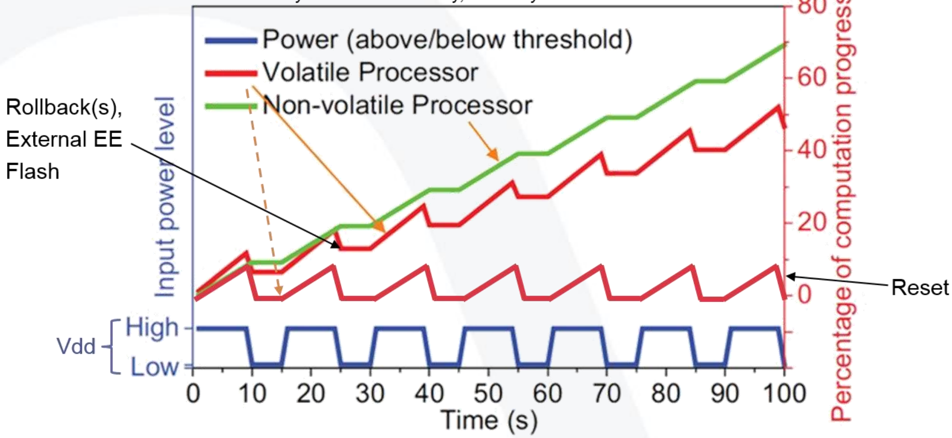
Distributed NV registers

NVP & NVS advantages

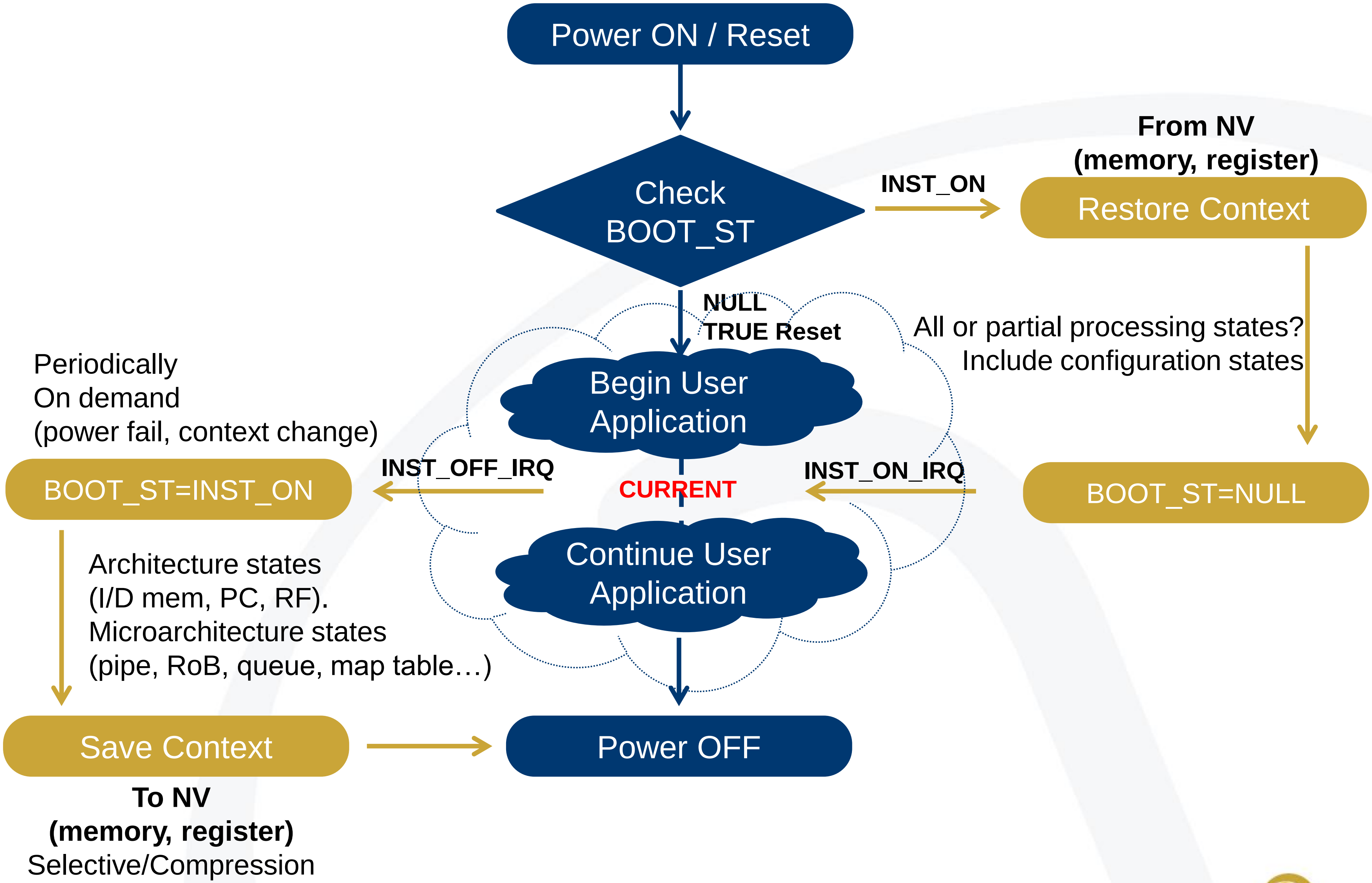
- Increase battery life
  - Instant ON/OFF → minimize SoC boot energy loss
  - Normally-OFF → no idle power consumption (power down)
- Intermittent power supply support
  - Harvesting
  - Avoid rollback
- Simplify sleep modes → simplify code dev.
- Simplify code maintenance
  - Flexible memory partitioning
  - Update over-the-air
- Multi-application support
  - Instant context switching
  - Reduced context saving overhead



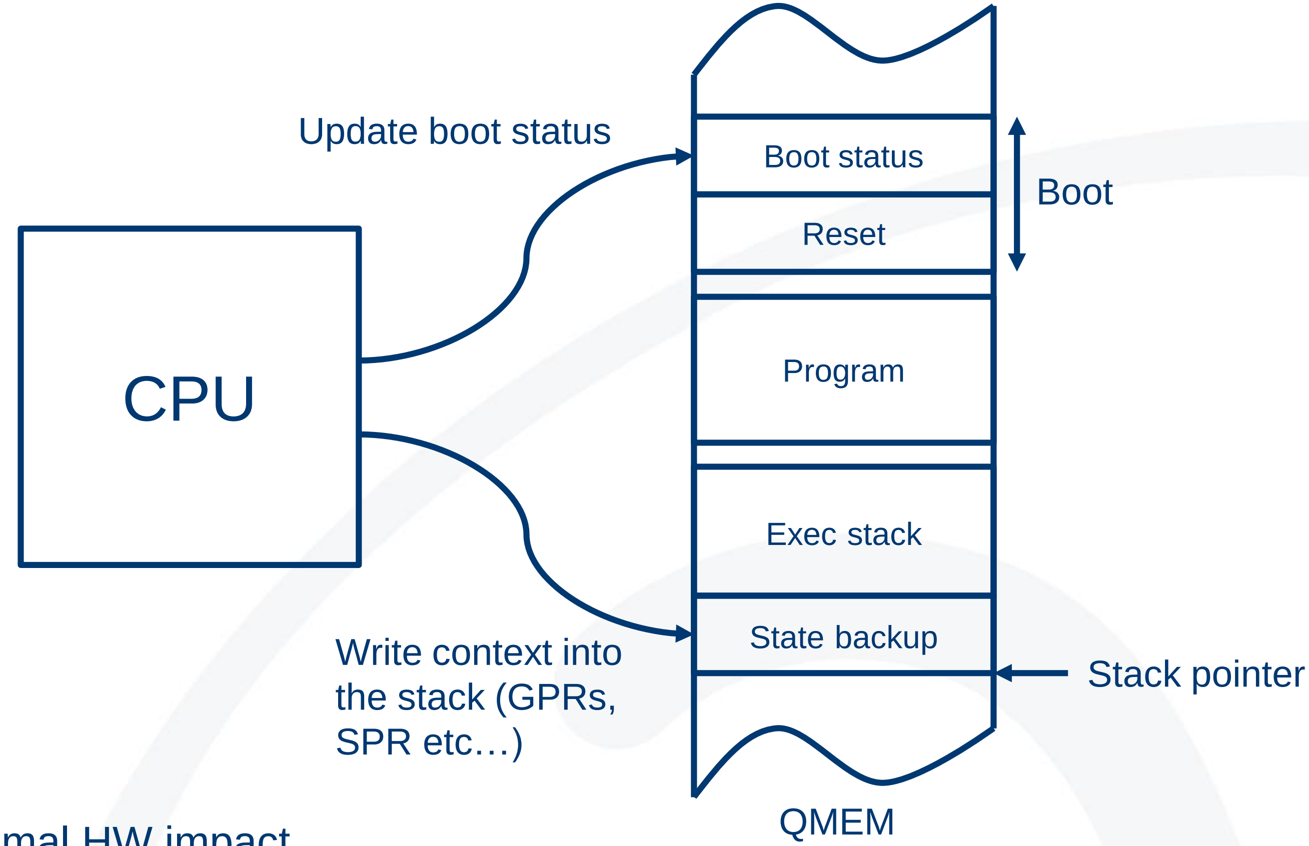
Source: Pennsylvania State University, University of California



NV CPU and System



SW retention state



+ Minimal HW impact

- Requires an API → more validation

- Requires memory protection

- Energy cost state dependent

- Duration state dependent → Not suitable for RT applications

- Complications with caches

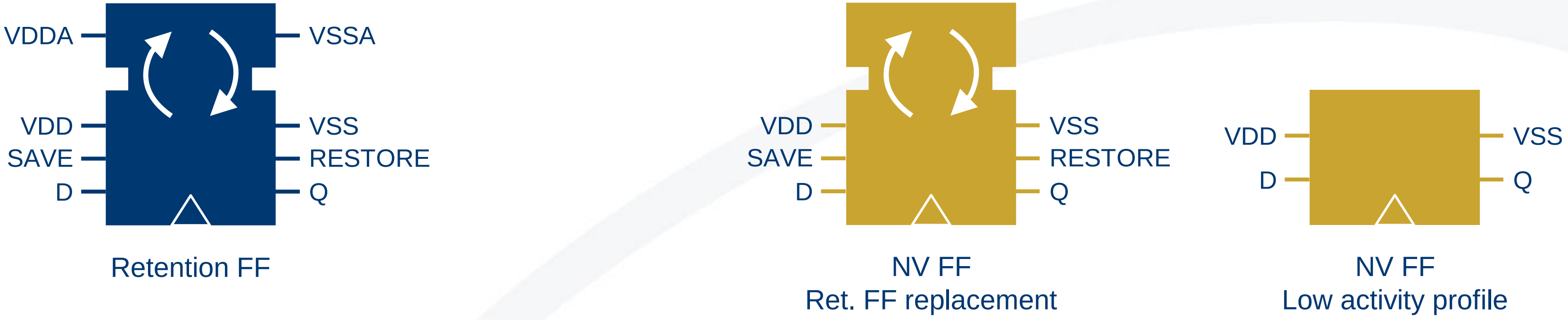
HW Retention state

- Existing approaches:
  - Retention FF: most efficient but largest
  - Scan-chain based approach:
    - uses existing scan-chain hardware
    - minimal area cost but slow and more power consuming
    - Complex (flow/dft)
  - Drowsy state retention:
    - freeze and reduce voltage
    - lowest area cost but least efficient
    - Complex power management (analog)

- Limitations:
  - Leakage overhead
  - Not power failure tolerant
  - Area overhead
  - HW impact + controller → extra verification

HW Retention state

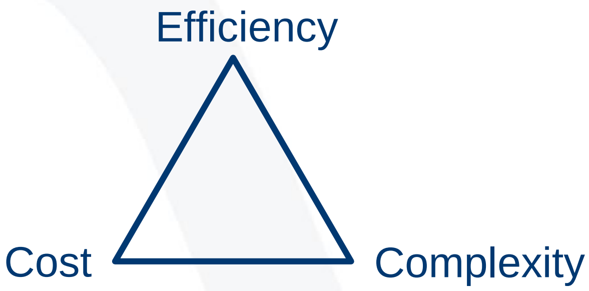
- Our approach: NV-FF (extend Retention FF)



- Advantages over existing approach:
  - Limited area overhead
  - No extra leakage
  - Power failure tolerant

- Partial vs Full replacement
  - Reduces area and energy overhead
  - Requires detailed knowledge of the design

  → Find best trade-off



Summary

THE COMPANY

THE CONTEXT

THE TECHNOLOGY

THE SYSTEM

THE CO-DEVELOPMENT

CONCLUSION

Hybridization

HP STTRAM

☺ vs SRAM

- Zero leakage at bit cell level
- Immune to power failure
- Immune to SEU

☹ vs SRAM

- Write/read power
- Write/read latency
- Limited endurance

SRAM

☺ vs STTRAM

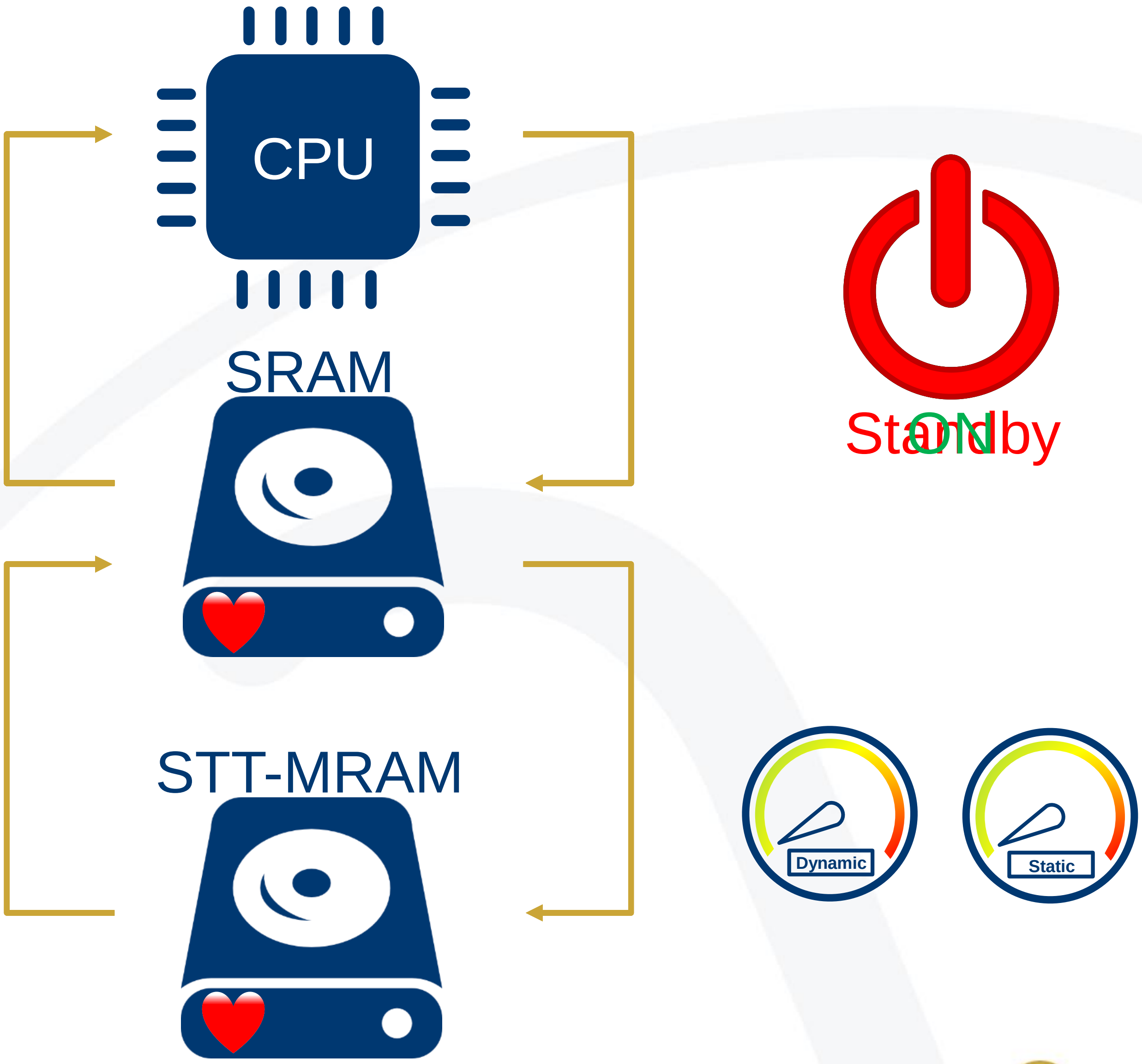
- Write/read power
- Write/read latency (CPU f.)
- Infinite endurance

☹ vs STTRAM

- µA/Mb of leakage at RT
- Not immune to power failure
- Not immune to SEU

« But how to efficiently exchange data between the two technologies with near instant-on/off capabilities ? »

NVSRAM



NVSRAM level

Hybridization at **bit cell level**

- ☺ Massives parallels (save/restore) transfers (fast)
- ☺ Energy-efficient transfers
- ☹ The largest area / SRAM bit cell/array adaptation
- ☹ Impact on SRAM read/write power and latency

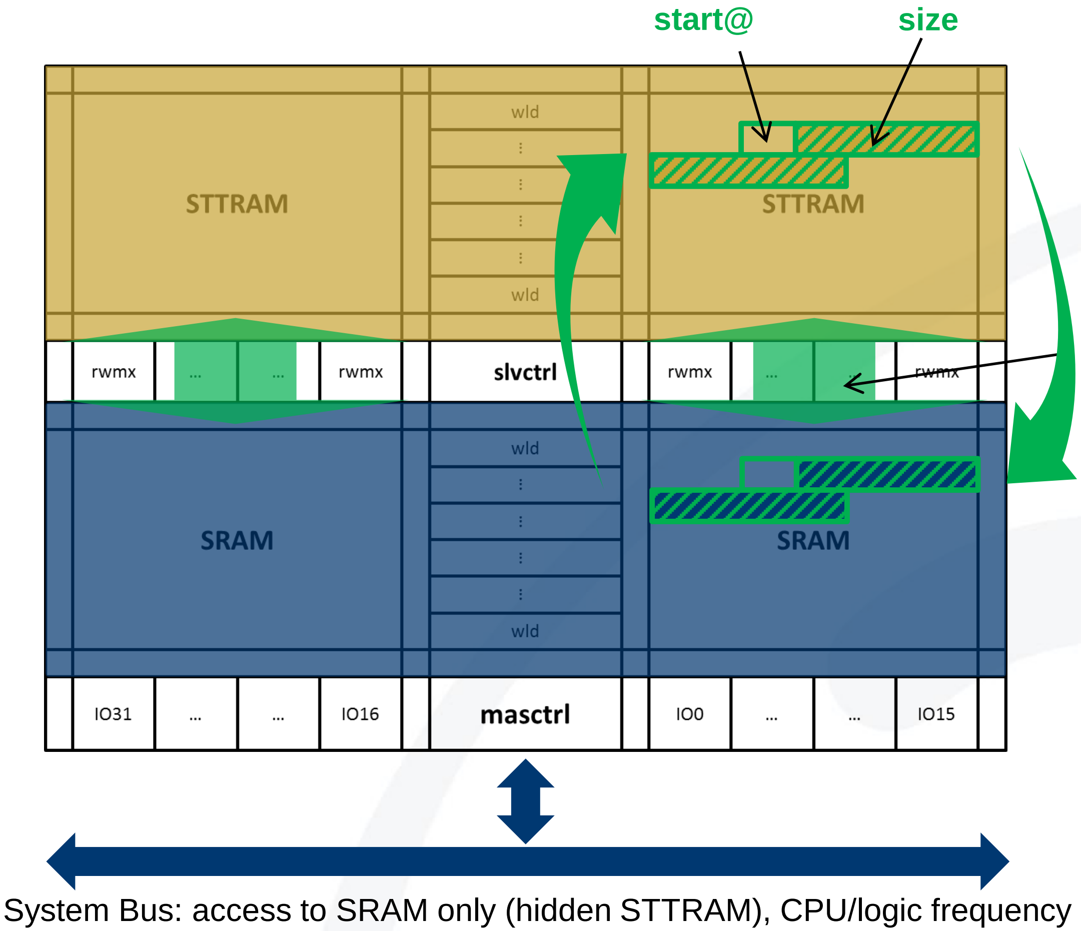
Hybridization at **IP level**

- ☺ Significant parallels (save/restore) transfers (fast)
- ☺ Energy-efficient transfers
- ☺ The smallest area
- ☺ No impact on SRAM

Hybridization at **system level**

- ☹ Limited parallels (save/restore) transfers (slow)
- ☹ Not energy-efficient transfers / complex routing
- ☺ Acceptable area
- ☺ No impact on SRAM

NVSRAM architecture

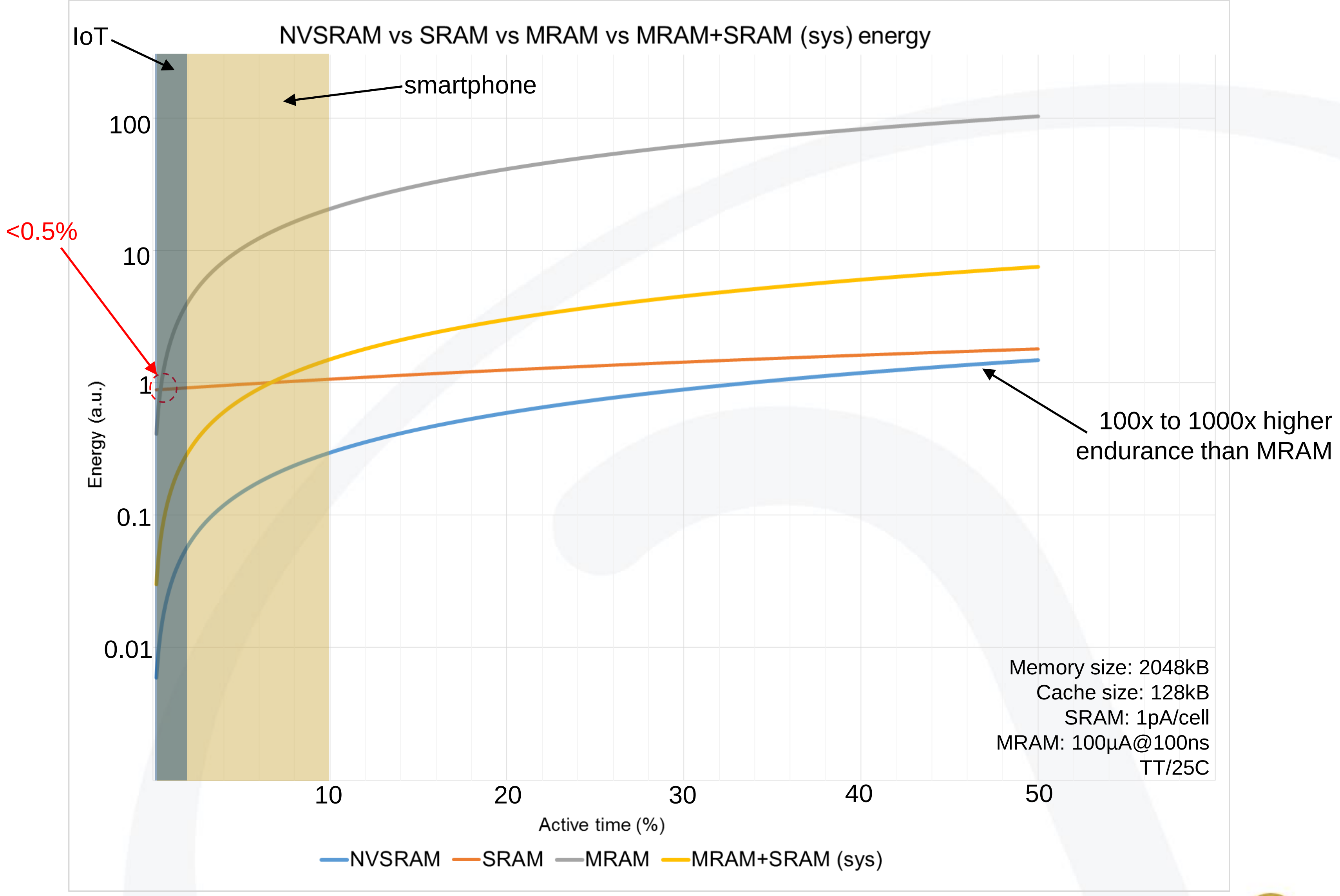


System Bus: access to SRAM only (hidden STTRAM), CPU/logic frequency

Internal Wide Bus:

- Transfers between SRAM and STTRAM
- Asynchronous
- Low power
- High bandwith

NVSRAM



100x to 1000x higher endurance than MRAM

Memory size: 2048kB
Cache size: 128kB
SRAM: 1pA/cell
MRAM: 100µA@100ns
TT/25C

Summary

THE COMPANY

THE CONTEXT

THE TECHNOLOGY

THE SYSTEM

THE CO-DEVELOPMENT

CONCLUSION

Conclusion

THE TECHNOLOGY

- Non-Volatile
- Power efficient
- Flexible

THE SYSTEM

- Normally-OFF
- Instant ON/OFF

THE CO-DEVELOPMENT

- Hybrid memory
- Increase efficiency

Find the best trade-off for the application

eVaderis

THANK
YOU
GRACIAS
ARIGATO
SHUKURIA
DANKSCHEEN
BIYAN
SHUKRIA
TINGKI
YAQHANYELAY
TASHAKKUR ATU
SUKSAMA
EKHMET
GRAZIE
MEHRBANI
MAAKE
KOMAPSUMNIDA
PALDIES
GOZAIMASHITA
EFCHARISTO
USPAXAR
BOLZÏN
MERCI